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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/869,397  | 06/28/2001  | Claude Chapel        | PF 980092           | 4292             |
| 7590  | 02/01/2006  |                      | EXAMINER            |                  |
| Joseph S Tripoli<br>Thomson Multimedia Licensing Inc<br>CN 5312<br>Princeton, NJ 08543-0028 |             |                      |                     | SHIBRU, HELEN    |
|   |             | ART UNIT             | PAPER NUMBER        | 2616             |

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                        |                     |  |
|------------------------------|------------------------|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |  |
|                              | 09/869,397             | CHAPEL ET AL.       |  |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |  |
|                              | HELEN SHIBRU           | 2616                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 08 November 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-8 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 28 June 2001 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____ .  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ .   | 6) <input type="checkbox"/> Other: _____ .                                  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendments, filed 11/08/2005, have been entered and made of record. Claims 1-8 are pending.

### ***Response to Arguments***

2. Applicant's arguments filed 06/13/05 have been fully considered but they are not persuasive.

In re page 3, Applicant states "Thomason describes a process for recording a digital video and audio data stream wherein recording is carried out on a medium (hard disk 36) organized In the form of logic blocks in series and comprising a recording and (reading head (column 4 line 36), the process comprising the steps of storing first in a buffer memory (35) the data before transferring them to the main memory (36) and also, when reading data on the main memory (36), data is initially sent to the buffer memory (35). The invention proposes a useful arrangement of the buffer memory in order to make the data transfers with the main memory using an efficient manner. However, the arrangement is dedicated to the management of the buffer memories and not to the arrangement of the main memory."

In response, the Examiner respectfully disagrees. Firstly, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. The argument is not reflecting the main language. Furthermore the main memory and the buffer

memory are not distinguishable. The buffer is arranged in order to manage the main memory to record and read the data (see col. 4 lines 43-51). In addition buffer is a medium.

In re page 3, Applicant states “Thomason the blocks are not arranged in logic blocks in buffers”.

In response, the Examiner respectfully disagrees. Thomason discloses blocks are arranged in logic blocks in buffer (see col. 5 line 41-col. 6 line 30). There is no difference between the blocks in fig. 3b, blocks P1 and P2, and logic block. Furthermore claim 1 does not recite ‘logic block in buffer’.

In re page 3, Applicant states “Thomason fails to teach, suggest or make obvious that the buffer is arranged by recording one address out of two starting from a first address, as claimed by at least the Applicant's independent claim 1.”

In response, the Examiner respectfully disagrees. Firstly, Thomason anticipates not make obvious since the examiner rejected under 35 U.S.C. 102. In addition, in a digital memory every block corresponds to address. Furthermore Thomason discloses all memory blocks includes a memory space for a pointer location that points to the address (see col. 5 lines 13-26). In addition claim 1 does not recite an address or ‘recording one address out of two starting from first address’. Please argue or refer to the claim language when arguing not based on the specification. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

In re page 3 last two lines and first two lines of page 4, Applicant states "Thomason also only discloses normal buffer management and not buffer management as taught in the Applicant's Specification and claimed by at least the Applicant's independent claim 1".

In response, the Examiner respectfully disagrees. Claim 1 does not recite buffer management and the examiner does not see the difference between normal buffer management and buffer management. As stated above the argument is not reflecting the claim language. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

In re page 4, Applicant states "Thomason fails to teach, suggest or anticipate 'recording data in one block out of two starting from a first block, following the triggering of the reading of the data, alternatively of reading a previously recorded block and of continuing the recording in the block following the block read'".

In response, the Examiner respectfully disagrees. In fig 3b two blocks are shown P1 and P2 (or 60). Data is recorded starting from the first block P2 and this block will be read first. Following the triggering of the reading of the data, alternatively of reading a previously recorded block, P1 will be read. Reading and recording of the data will continue in FIFO and LIFO. Oldest block will be out first and most recent block will be last in (see fig. 1, 3a, 3b, 4 and col. 4 lines 47-51, col. 5 lines 1-64).

The examiner believes that the claimed invention does in fact read on the cited references for at least the reasons discussed above and as stated in the detail Office Action as follows. This Office action is now made final.

***Claim Rejections - 35 USC § 102***

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-4, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Thomason (US Pat. No. 6,018,612).

Regarding claim 1, Thomason discloses a process for recording a digital video and audio data stream wherein recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head (see col. 4 lines 36-40 and col. 5 lines 13-15), said process comprises the steps of:

recording data in one block out of two starting from a first block (see col. 4 lines 47-51, col. 5 lines 7-26, and fig. 3 (60)),

following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read (see col. 4 lines 52-67).

Regarding claim 2, Thomason discloses when the set of blocks recorded before the triggering of reading have been read, recording is continued in contiguous blocks in a non-interlaced manner (see col. 5 lines 5-15, P1 and P2).

Regarding claim 3, Thomason discloses when the set of blocks recorded before the triggering of reading have been read, recording is continued in a loop in the blocks previously

read (see col. 5 lines 48-57 and fig. 3 first recording is in block 51a and reading is in block 59a, oldest block (first out) (recording) and most recent block (last in) (reading), after reading is triggered in 51a (first out) and recording is continued in 59a, and the recording and reading loop is continued).

Regarding claim 4, Thomason discloses when the set of blocks recorded before the triggering of reading have been read, said blocks are read, then rewritten in a non-interlaced manner (see col. 5 lines 48-52, it is inherent that the reading and recording is done in a non-interlaced manner).

Regarding claim 6, Thomason discloses an additional step of, detecting sequences of free blocks on the medium and of applying steps of recording and of reading inside such sequences (see col. 5 lines 10-13 it is inherent that the free blocks are detected and the pointers pointed to those blocks).

Regarding claim 7, Thomason discloses a digital television receiver (see fig. 1 signals in and col. 3 lines 40-46) comprising means for receiving a digital audio and video data stream (see col. 4 lines 13-32), comprising:

a recording medium furnished with a recording and reading head, said medium being organized in the form of logic blocks in series (see col. 4 lines 36-40);

a control circuit (see fig. 3 control block (60)) for managing the writing and the reading of blocks of the recording medium (see col. 5 lines 5-10);

an interfacing circuit (see fig. 1 user interface device (26)) for interfacing the recording medium with said control circuit (see col. 3 lines 60-67), said control circuit initially instructing the recording of data in one block out of two starting from a first block and subsequently (see

col. 5 lines 5-10), following the triggering of the reading of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read (see col. 4 lines 52-67).

***Claim Rejections - 35 USC § 103***

6. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomason in view of Mishara (US Pat. No. 6,304,927).

Regarding claim 5, claim 5 differ from Thomason in that the claim further requires the recording of data is performed in a group of N contiguous blocks ( $N > 1$ ) out of two instead of a single block out of two. Although Thomason does not specifically discloses the recording of data is performed in a group of N contiguous blocks ( $N > 1$ ) out of two instead of a single block out of two, Thomason discloses memory blocks are chained and they include memory space (see col. 5 lines 11-15). Thomason further discloses memory blocks are added to the queue at the end of the chain (see col. 5 lines 26-29).

In the same field of endeavor, Mishara discloses a DMA (direct memory acces) transfers are performed in blocks (see col. 5 lines 15-19). Mishara further discloses the size of the DMA transfers and the buffers used are chosen based on the system architecture (see col. 5 lines 25-30). Mishara further disclose for a 32-byte DMA buffer the block sizes are 16 bytes (see col. 5 lines 42-48, two 16 byte blocks for 32 byte DMA buffer). Therefore in light of the teaching in Mishara it would have been obvious to modify Thomason DMA buffer size in order to transfer images efficiently.

Claim 8 is rejected for the same reason as discussed in claim 5 above.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

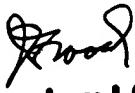
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELEN SHIBRU whose telephone number is (571) 272-7329. The examiner can normally be reached on M-F, 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAMES J. GROODY can be reached on (571) 272-7950. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Helen Shibru  
January 6, 2006

  
James J. Grody  
Supervisory Patent Examiner  
Art Unit 262 2616